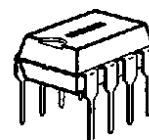


Nonvolatile Memory 2-Kbit E²PROM with I²C Bus and 2 K Write Protection

SDA 3526
MOS IC

Features

- Word-organized programmable nonvolatile memory in n-channel floating-gate technology (E²PROM)
- 256 × 8-bit organization
- Supply voltage 5 V
- Serial 2-line bus for data input and output (I²C Bus)
- Reprogramming mode, 10 ms erase / write cycle
- Reprogramming by means of on-chip control (without external control)
- Check for end of programming process
- Programming protect mode
- Data retention > 10 years
- More than 10⁵ reprogramming cycles **per address**



P-DIP-8-4



P-DSO-8-1

Type	Ordering Code	Package	Pin Configuration
SDA 3526-5	Q67100-H3254	P-DIP-8-4	SIEMENS
SDA 3526-5 A2G	Q67100-H5092	P-DSO-8-1 (SMD)	SIEMENS

Circuit Description

I²C Bus Interface

The I²C Bus is a bidirectional 2-line bus for the transfer of data between various integrated circuits. It consists of a serial data line SDA and a serial clock line SCL. The data line requires an external pull-up resistor to V_{CC} (open drain output stage).

The possible operational states of the I²C Bus are shown in **figure 1**. In the quiescent state, both lines SDA and SCL are high, i.e. the output stage of the data line is disabled. As long a SCL remains "1", information changes on the data bus indicate the start or the end of data transfer between two components.

The transition on SDA from "1" to "0" is a start condition, the transition from "0" to "1" is a stop condition. During a data transfer the information on the data bus will only change while the clock line SCL is "0". The information on SDA is valid as long as SCL is "1".

In conjunction with an I²C Bus system, the memory component can operate as a receiver and as a transmitter (slave receiver or slave transmitter). Between a start and stop condition, information is always transmitted in byte-organized form. Between the falling edge of the eighth clock pulse and a ninth acknowledge clock pulse, the memory component sets the SDA-line to low as a confirmation of reception, if the chip select conditions have been met. During the output of data, the data output of the memory is high in impedance during the ninth clock pulse (acknowledge master).

The signal timing required for the operation of the I²C Bus is summarized in **figure 2**.

Control Functions of the I²C Bus

The memory component is controlled by the controller (master) via the I²C Bus in two operating modes: read-out cycle, and reprogramming cycle, including erase and write to a memory address. In both operating modes, the controller, as transmitter, has to provide 3 bytes and an additional acknowledge clock pulse to the bus after the start condition. During a memory read, at least nine additional clock pulses are required to accept the data from the memory and the acknowledge master, before the stop condition may follow. In the case of programming, the active programming process is only started by the stop condition after data input (**see figure 3**).

The chip select word contains the 3 chip select bits CS0, CS1 and CS2, thus allowing 8 memory chips to be connected in parallel. Chip select is achieved when the three control bits logically correspond to the selected conditions at the select inputs.

Check for End of Programming or Abortion of Programming Process

If the chip is addressed during active reprogramming by entering CS/E, the programming process is terminated. If, however, it is addressed by entering CS/A, the entry will be ignored. Only after programming has been terminated will the chip respond to CS/A. This allows the user to check whether the end of the programming process has been reached (**see figure 3**).

Memory Read

After the input of the first two control words CS/E and WA, a resetting of the start condition and the input of the third control word CS/A, the memory is set ready to read. During acknowledge clock nine, the memory information is transferred in parallel mode to the shift register. Subsequent to the falling edge of the acknowledge clock, the data output is low impedance and the first data bit can be sampled (**see figure 4**).

With every shift clock, an additional bit reaches the output. After reading a byte, the internal address counter is automatically incremented when the master receiver switches the data line to "low" during the ninth clock (acknowledge master). Any number of memory locations can thus be read one after the other. At address 256, an overflow to address 0 is initiated. With the stop condition, the data output returns to high-impedance mode. The internal sequence control of the memory component is reset from the read to the quiescent state with the stop condition.

Memory Reprogramming

The reprogramming cycle of a memory word comprises an erase and a subsequent write process. During erase, all eight bits of the selected word are set into the "1" state. During write, "0" states are generated according to the information in the internal data register, i.e. according to the third input control word. After the 27th and last clock of the control word input, the active programming process is started by the stop condition. The active reprogramming process is executed under on-chip control.

The time required for reprogramming depends on component deviation and data patterns. Therefore, with rated supply voltage, the erase/write process extends over max. 20 ms, or more typically, 10 ms. In the case of data word input without write request (write request is defined as data bit in data register set to "0"), the write process is suppressed and the programming time is shortened. During a subsequent programming of an already erased memory address, the erase process is suppressed again, so that the reprogramming time is also shortened.

Important: Switch-On Mode and Chip Reset

After the supply voltage V_{CC} has been connected, the data output will be in high-impedance mode. As a rule, **the first operating mode** to be entered, should be the **read process of a word address**. As a result of the built-in "power-on reset" circuit, programming requests will not be accepted immediately after the supply voltage has been switched on.

Total Erase

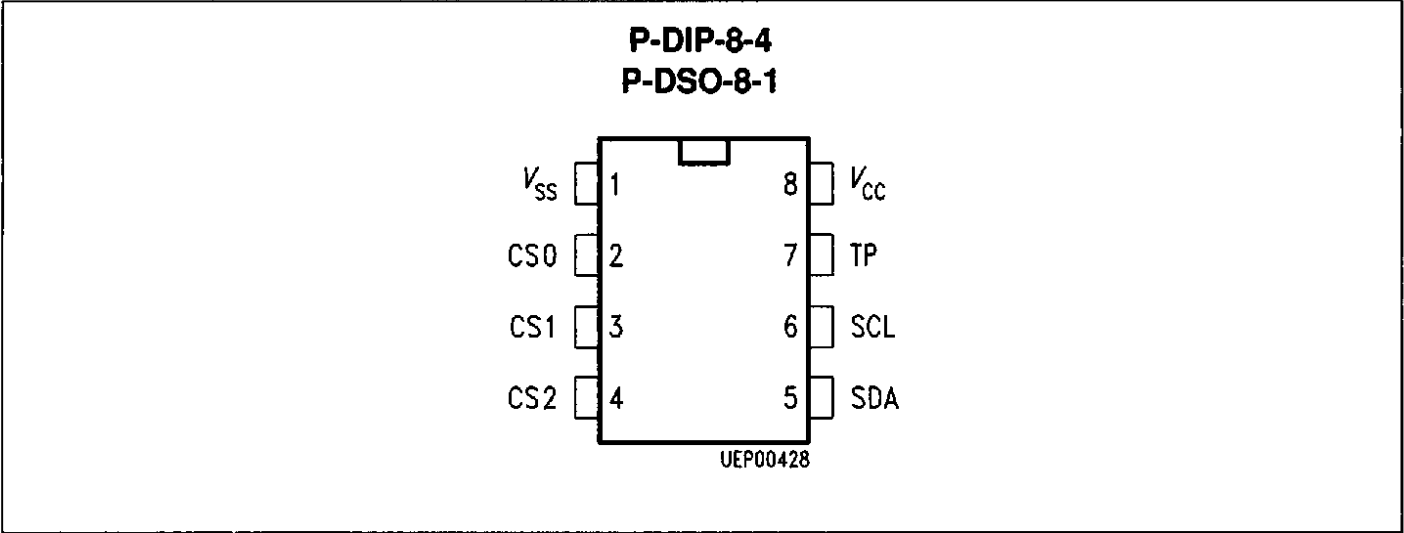
Enter the control word CS/E, load the address register with address 0 and the data register with FF (hex) to erase the entire contents of the memory. Switch input CS2 to "open" immediately prior to generating the stop condition. The subsequent stop condition triggers a total erase. Upon termination of "total erase", CS2 must be reconnected to either 0 V or ≥ 4.5 V.

Programming Protect Mode

When pin 2 is not connected, i. e. when CS0 is floating, this means that:

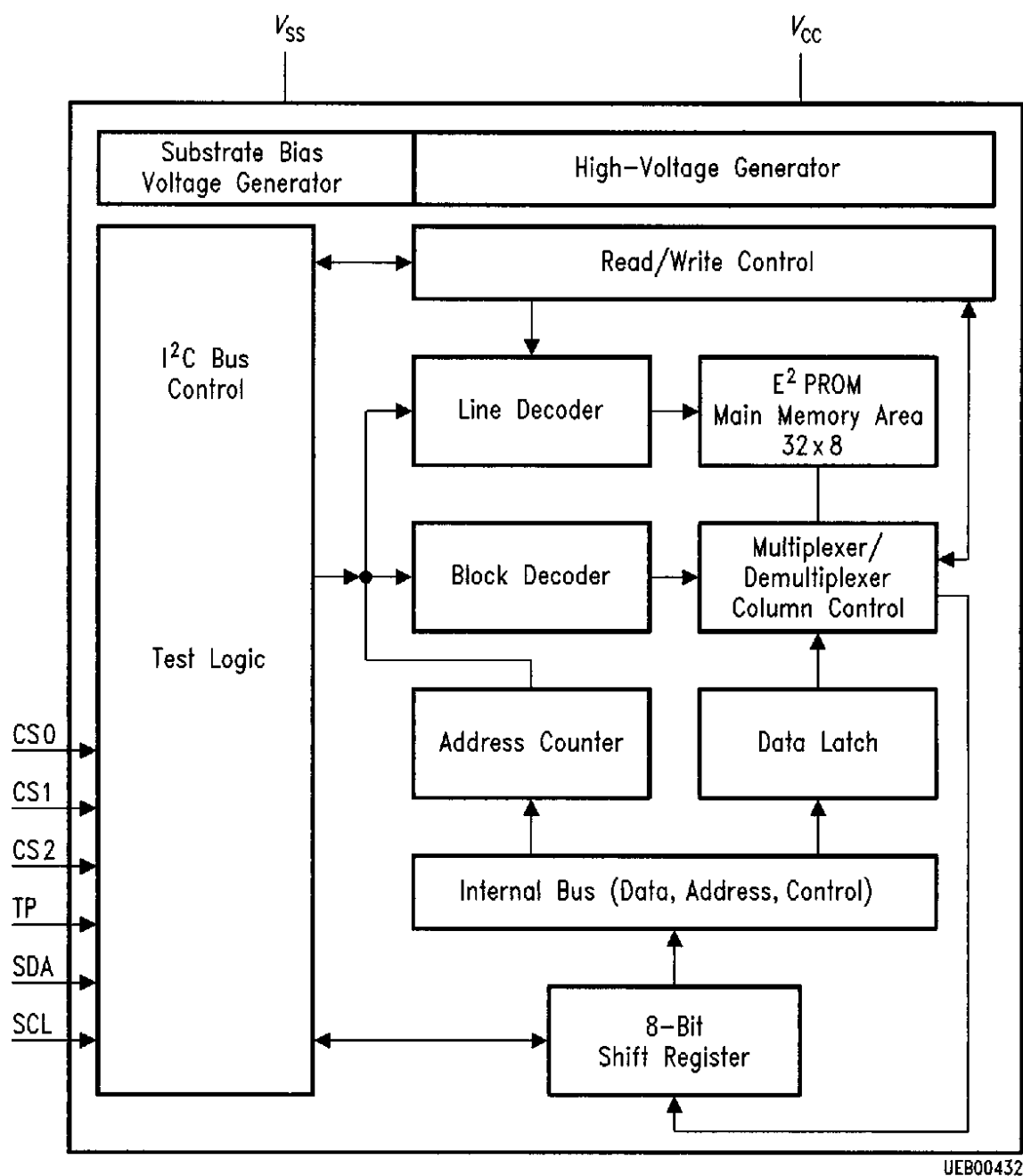
- 1) memory reprogramming is disabled for addresses 0 ... 255.
- 2) the chip can only be addressed with chip select bit CS0 = 0 of control word CS/E or CS/A.

Pin Configuration
(top view)



Pin Definitions and Functions

Pin No.	Symbol	Function
P-DIP-8-4 / P-DSO-8-1		
1	V_{SS}	Ground
2	CS0	Chip select $0 \leq V_I \leq 0.2\text{ V}$; $4.5 \leq V_I \leq V_{CC}$, open, programming disabled condition (addresses 0 ... 255)
3	CS1	Chip select
4	CS2	Chip select $0 \leq V_I \leq 0.2\text{ V}$; $4.5 \leq V_I \leq V_{CC}$, open, total erase condition
5	SDA	Data line
6	SCL	Clock line
7	TP	Test pin
8	V_{CC}	Supply voltage



Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_{CC}	− 0.3	6	V
Input voltage	V_I	− 0.3	6	V
Power dissipation	P_D		130	mW
Storage temperature	T_{stg}	− 40	125	°C
Thermal resistance (system-air)	$R_{th\ SA}$		100	K/W
Junction temperature	T_j		85	°C

Operating Range

Supply voltages	V_{CC}	4.75	5.25	V
Ambient temperature	T_A	0	70	°C

Characteristics $T_A = 25\text{ }^{\circ}\text{C}$

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply voltage	V_{CC}	4.75	5.0	5.25	V	
Supply current	I_{CC}			20	mA	$V_{CC} = 5.25\text{ V}$

Inputs

Input voltages SDA/SCL	V_{IL}			1.5	V	
Input voltages SDA/SCL	V_{IH}	3.0		V_{CC}	V	
Input currents SDA/SCL	I_{IH}			10	μA	$V_{IH} = V_{CC}$

Outputs

Output current SDA	I_{QL}			3.0	mA	$V_{QL} = 0.4\text{ V}$
Leakage current SDA	I_{QH}			10	μA	$V_{QH} = V_{CC\text{ max}}$

Inputs

Input voltages CS0/CS1/CS2	V_{IL}			0.2	V	
Input voltages CS0/CS1/CS2	V_{IH}	4.5		V_{CC}	V	
Input currents CS0/CS1/CS2	I_{IH}			100	μA	$V_{CC} = 5.25\text{ V}$
Clock frequency	f_{SCL}			100	kHz	
Reprogramming duration	t_{PROG}		10	20	ms	erase and write
Input capacity	C_I			10	pF	
Total erase	t_{GL}			20	ms	CS2 = open

Diagrams

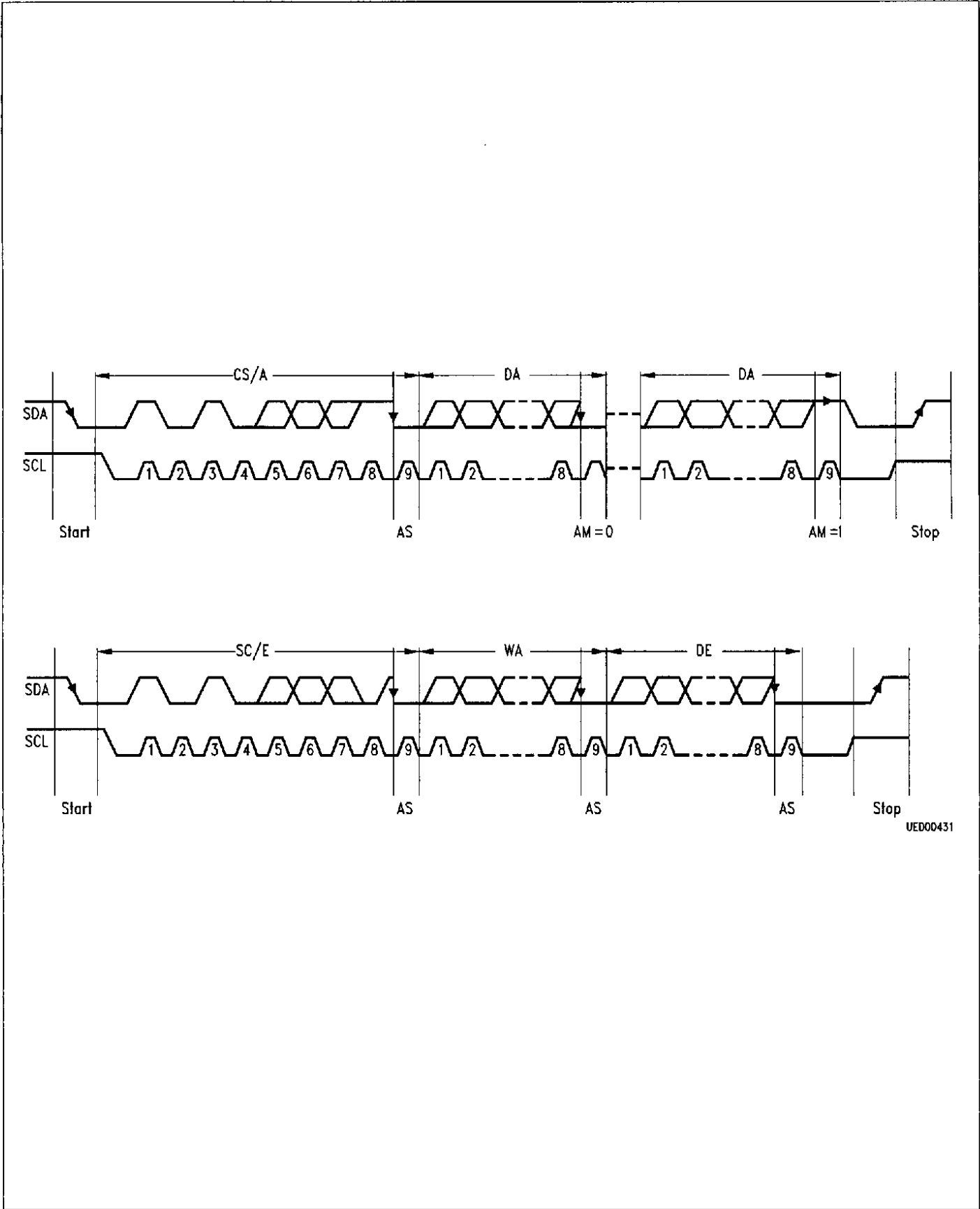


Figure 1
Operation States of the I²C Bus

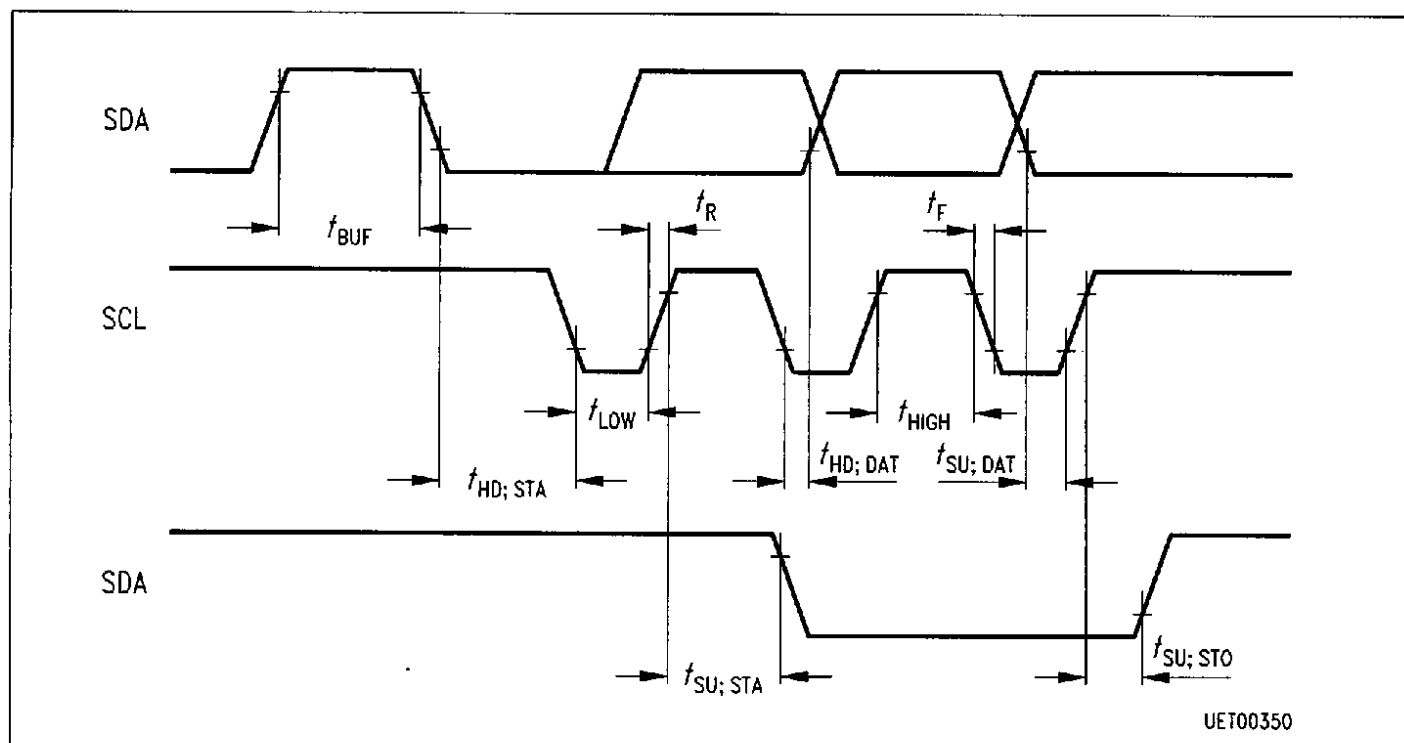


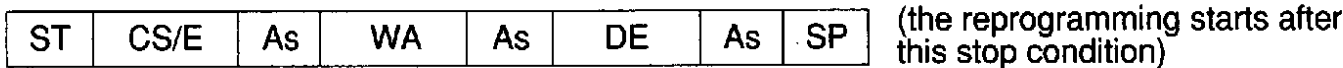
Figure 2
Timing Conditions for the I²C Bus

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Minimum time the bus must be free before a new transmission can start	t_{BUF}	4.7		μs
Start condition hold time	$t_{HD; STA}$	4.0		μs
Clock low period	t_{LOW}	4.7		μs
Clock high period	t_{HIGH}	4.0		μs
Start condition set-up time, only valid for repeated start code	$t_{SU; STA}$	4.7		μs
Data set-up time	$t_{SU; DAT}$	250		ns
Rise time of both the SDA and SCL line	t_R		1	μs
Fall time of both the SDA and SCL line	t_F		300	ns
Stop condition set-up time	$t_{SU; STO}$	4.7		μs
Hold time data	$t_{HD; DAT}$	0*)		

*) Note that a transmitter must internally provide at least a hold time to bridge the undefined region (max. 300 ns) of the falling edge of SCL.

Figure 3
Programming

Control word input



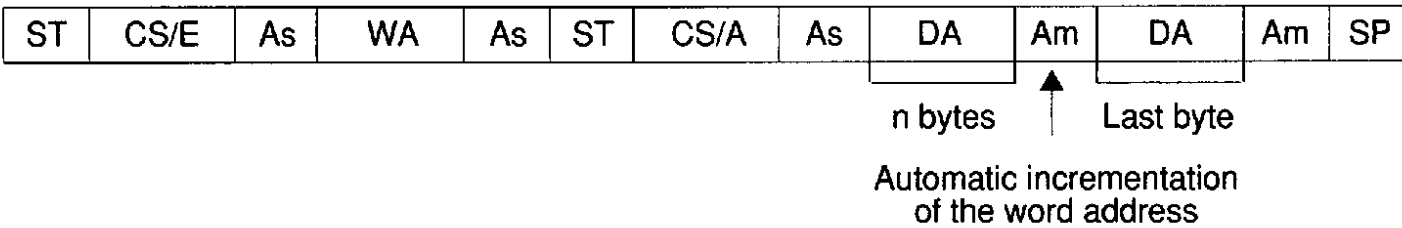
- 1. when As = 1 programming is not terminated
- 2. when As = 0 programming is terminated



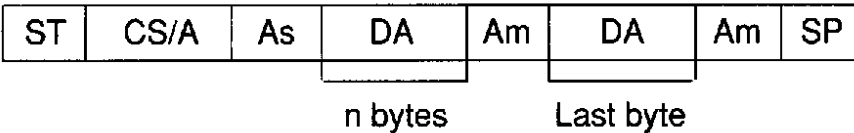
Figure 4
Read

Control word input read

a) complete (with word address input)



b) shortened:
Bit 0 ... 7 the last selected word address remain unchanged



Autoincrement Am = 0
Prior to stop condition Am = 1

Control Word Table

Clock No.	1	2	3	4	5	6	7	8	9	(Acknowledge)
CS/E	1	0	1	0	CS2	CS1	CS0	0	0	through memory
CS/A	1	0	1	0	CS2	CS1	CS0	1	0	through memory
WA	A7	A6	A5	A4	A3	A2	A1	A0	0	through memory
DE	D7	D6	D5	D4	D3	D2	D1	D0	0	through memory
DA	D7	D6	D5	D4	D3	D2	D1	D0	0/1	through master

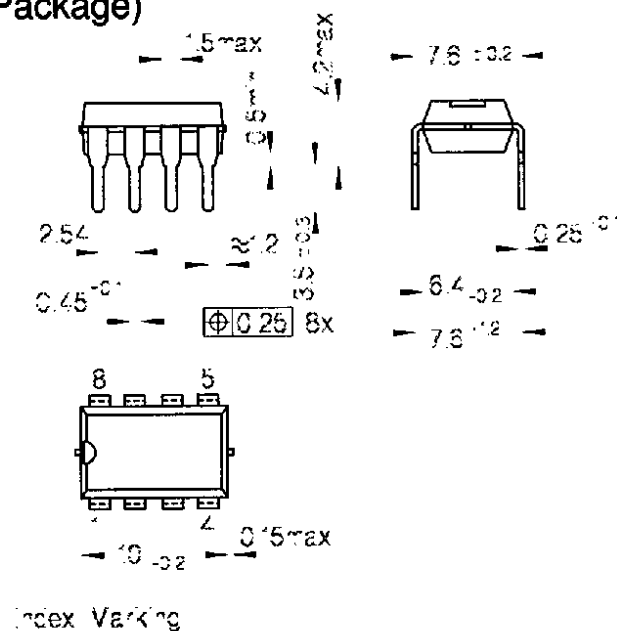
Control Word Input Key

CS/E	Chip select for data input into memory
CS/A	Chip select for data output out of memory
WA	Memory word address
DE	Data word for memory
DA	Data word read out of memory
D0 to D7	Data bits
ST	Start condition
SP	Stop condition
As	Acknowledge bit from memory
Am	Acknowledge bit from master
CS0, CS1, CS2	Chip select bits
A0 to A7	Memory word address bits

3 Package Outlines

P-DIP-8-4

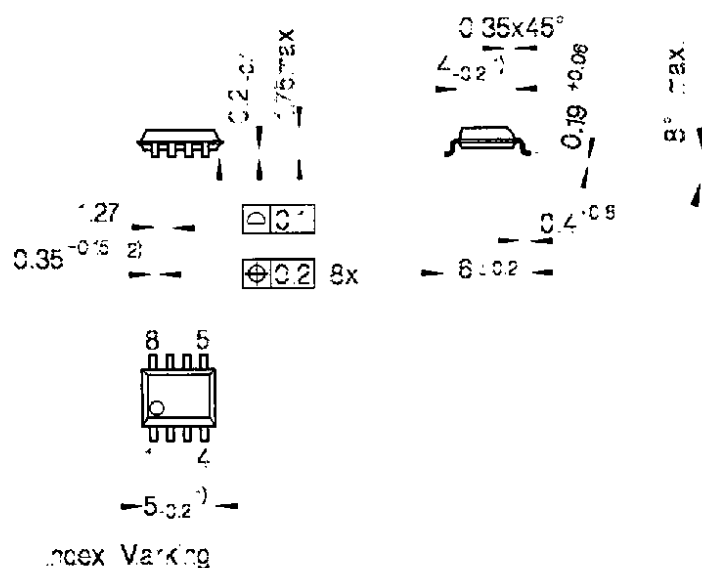
(Plastic Dual In-line Package)



GPD05025

P-DSO-8-1

(Plastic Dual Small Outline Package)



- 1) Does not include plastic or metal protrusion of 0.15^{max} per side
- 2) Does not include dambar protrusion of 0.05^{max} per side

GPS05121

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD - Surface Mounted Device

Dimensions in mm

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Siemens AG Österreich
Erdberger Lände 26
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☎ (01) 71711-56 11
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AUS

Siemens Ltd., Head Office
544 Church Street
Richmond (Melbourne), Vic. 3121
☎ (03) 4207111
☎ 30425
Fax (03) 4207275

B

Siemens Electronic Components
Benelux
Charleroisesteenweg 116/
Chaussée de Charleroi 116
B-1060 Brussel/Bruxelles
☎ (+32) 2-536 23 48
Fax (+32) 2-536 28 57

BR

ICOTRON S.A.
Indústria de Componentes
Eletrônicos
Avenida Mutinga, 3650-6ª andar
05150 São Paulo-SP
☎ (011) 833-2211
☎ 11-81001
Fax (011) 831-4006

CDN

Siemens Electric Ltd.
Electronic Components Division
1180 Courtney Park Drive
Mississauga, Ontario L5T 1P2
☎ (416) 5641995
☎ (069) 68841
Fax (416) 670-6563

CH

Siemens-Albis AG
Freilagerstraße 28
8047 Zürich
☎ (01) 495-3111
☎ 823781-23
Fax (01) 495-5050

D

Siemens AG
Salzufer 6-8
10587 Berlin
☎ (030) 3993-26 26
Fax (030) 3993-24 90

Siemens AG
Lahnweg 10
40219 Düsseldorf
☎ (0211) 399-2930
Fax (0211) 399-14 81

Siemens AG
Lindenplatz 2
20099 Hamburg
☎ (040) 2889-27 85
Fax (040) 2889-30 96

Siemens AG
Werner-von-Siemens-Platz 1
30880 Laatzen (Hannover)
☎ (0511) 877-22 22
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Fax (0711) 137 24 48

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Siemens A/S
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☎ 1258 222
Fax 44 77 4017

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Siemens S.A.
Dpto. Componentes
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28760 Tres Cantos-Madrid
☎ (01) 803 00 85
Fax (01) 803 39 26

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Siemens S.A.
39/47, Bd. Ornano
93527 Saint-Denis CEDEX 2
☎ (1) 49 22 3100
☎ 234 077
Fax (1) 49 22 39 70

GB

Siemens plc
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Bracknell
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Fax (0344) 39 66 32

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Siemens AE
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P.O.B. 61011
15110 Amaroussio/Athen
☎ (01) 686 4111
☎ 216 292
Fax (01) 686 42 99

HK

Siemens Components Ltd
23/F., Tai Yau Building
181 Johnston Road, Wanchai
Hong Kong
☎ (852) 28 32 05 00
Fax (852) 28 27 84 21

I

Siemens S.p.A.
Semiconductor Sales
Via dei Valtorta, 48
20127 Milano
☎ (02) 66 76-1
Fax (02) 66 76-43 95

IND

Siemens Ltd.
Head Office
134-A, Dr. Annie Besant Road,
Worli
P.O.B. 6597
Bombay 400018
☎ (022) 4 93 87 86
☎ 1 175 142
Fax (022) 4 94 02 40

IRL

Siemens Ltd.
Electronic Components Division
8 Raglan Road
Dublin 4
☎ (01) 6 68 47 27
☎ 93 744
Fax (01) 68 46 33

J

Fuji Electronic Components Ltd
Shinjuku Koyama Bldg. 2F
30-3, 4-Chome
Yoyogi, Shibuya-ku
Tokyo 151
☎ (81) 3-53 88 85 25
Fax (81) 3-33 76 97 92

N

Siemens A/S
Østre Aker vei 90
Postboks 10, Veitvet
0518 Oslo 5
☎ (02) 63 30 00
☎ 78 477
Fax (02) 63 38 05

NL

Siemens Electronic Components
Benelux
Postbus 16068
NL-2500 BB Den Haag
☎ (+31) 70-333 24 29
Fax (+31) 70-333 28 15

P

Siemens S.A.
Estrada Nacional 117, Km 2,6
Alfragide
2700 Amadora
☎ (01) 417 00 11
☎ 62 955
Fax (01) 417 28 70

PL

Siemens Sp. z.o.o.
ul. Stawki 2
POB 276
00-950 Warszawa
☎ 6 35 16 19
☎ 825 554
Fax 6 35 52 38

RC

Tai Engineering Co., Ltd.
6th Fl., Central Building
108, Chung Shan North Road, Sec. 2
P.O. Box 68-1882
Taipei 10449
☎ (02) 5 23 47 00
☎ 27860 taiengco
Fax (02) 5 36 70 70

ROK

Siemens Ltd.
Asia Tower Bldg, 10th floor
726 Yeoksam-dong, Kangnam-ku
CPO Box 3001, Seoul 135-080
Korea
☎ (822) 5 27-77 40
Fax (822) 5 27-77 79

RUS

Siemens AG
1. Donskoj pr., 2
Moskva 117419
☎ (095) 2 37-64 76, -69 11
☎ 414 385
Fax (095) 2 37-66 14

S

Siemens Components
Österögatan 1
Box 46
S-164 93 Kista
☎ (08) 7 03 35 00
☎ 11 672
Fax (08) 7 03 35 01

SF

Siemens Oy
P.O.B. 60
02601 Espoo
☎ (0) 51 051, ☎ 124 465
Fax (0) 51 05 23 98

SGP

Siemens Components Pte. Ltd.
166 Kallang Way
Singapore 1334
☎ (65) 840 06 00
Fax (65) 742 10 80

TR

SIMKO Ticaret ve Sanayi A.S.
Meclisi Mebusan Cad. No. 125
P.K. 1001, 80007 Karaköy
80040 Findikli
☎ (01) 2 51 09 00
☎ 24 233 sies tr
Fax (01) 2 52 41 34

USA

Siemens Components, Inc.
Integrated Circuit Division
10950 North Tantau Avenue
Cupertino, CA 95014
☎ (408) 7 77-45 00
Fax (408) 7 77-49 77

ZA

Siemens Ltd.
Siemens House,
P.O.B. 4583
Johannesburg 2000
☎ (011) 3 15 19 50
☎ 450 091
Fax (011) 3 15 19 68