TDA2002 • TDA2002A

8 WATT AUDIO POWER AMPLIFIERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

4

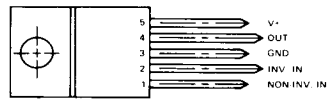
GENERAL DESCRIPTION – The TDA2002 and TDA2002A are monolithic integrated circuits designed for class B audio power amplifier applications using low impedance loads (down to 1.6 Ω). They are constructed using the Fairchild Planar* epitaxial process. The devices typically provide 8 W at 14.4 V, 2 Ω and 6.5 W at 16 V, 4 Ω.

The TDA2002 and TDA2002A are provided in a 5-pin power package, with two pin configurations (H and V) for ease in mounting either horizontally or vertically in the PC board.

The TDA2002A is the same electrically as the TDA2002 except it does not include the overvoltage (Load dump) protection circuit.

- **THERMAL SHUT DOWN**
- **SHORT CIRCUIT PROTECTION (AC)**
- **OVERVOLTAGE PROTECTION (TDA2002)**
- **LOW EXTERNAL COMPONENTS**
- **HIGH CURRENT CAPABILITY (3.5 A)**
- **MINIMUM SPACE REQUIREMENT**
- **WIDE SUPPLY VOLTAGE RANGE (8 V to 18 V)**

CONNECTION DIAGRAM
5-PIN POWER PACKAGE
(TOP VIEW)
PACKAGE OUTLINE GO
PACKAGE CODE H, V



ORDER INFORMATION

TYPE	PART NO.
2002H	TDA2002H
2002V	TDA2002V
2002AH	TDA2002AH
2002AV	TDA2002AV

ABSOLUTE MAXIMUM RATINGS

	TDA2002	TDA2002A
Peak Supply Voltage (50 ms)	40 V	---
Supply Voltage	28 V	28 V
Operating Supply Voltage	18 V	18 V
Output Current (Repetitive)	3.5 A	3.5 A
Output Current (Non-Repetitive)	4.5 A	4.5 A
Power Dissipation: at $T_C = 90^\circ C$	15 W	15 W
Storage Temperature	−40 to 150°C	−40 to 150°C
Pin Temperature (Soldering, 10 s)	260°C	260°C

THERMAL DATA

θ_{JC} Thermal resistance junction to case (max) 4°C/W

* Planar is a patented Fairchild Process.

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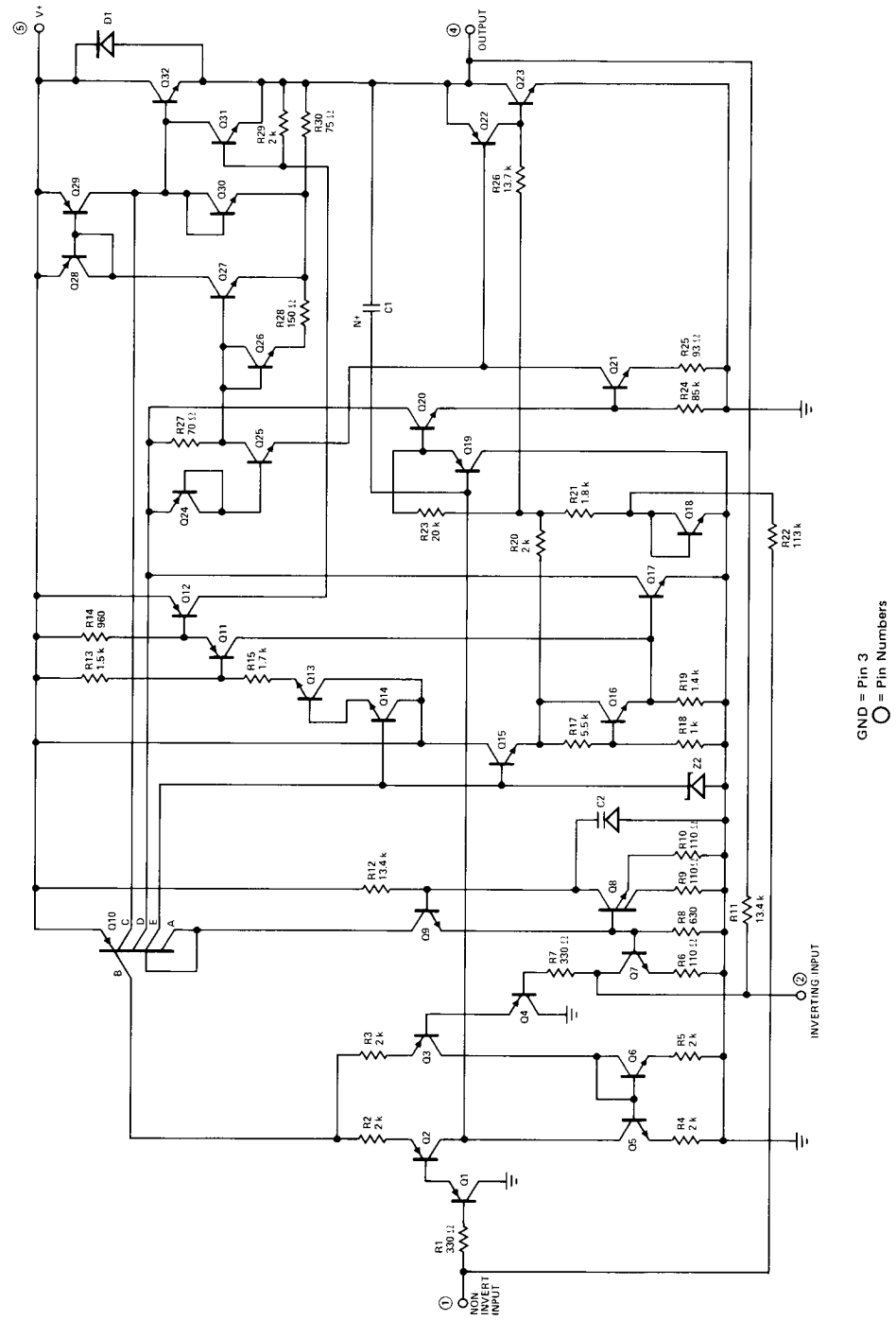
EQUIVALENT CIRCUIT



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ELECTRICAL CHARACTERISTICS: V+ = 14.4 V, T_A + 25°C, unless otherwise specified; see test circuit

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Output Voltage (Pin 4)		6.4	7.2	8.0	V
Quiescent Drain Current (Pin 5)			45	80	mA
Power Output	THD = 10% A_V = 100 f = 1 kHz				
	V+ = 16 V R_L = 4 Ω		6.5		W
	V+ = 16 V R_L = 2 Ω		10		W
	V+ = 14.4 V R_L = 4 Ω	4.8	5.2		W
	V+ = 14.4 V R_L = 2 Ω	7	8		W
Input Saturation Voltage (rms)		600			mV
Input Sensitivity	A_V = 100 f = 1 kHz				
	P_{OUT} = .5 W R_L = 4 Ω		15		mV
	P_{OUT} = .5 W R_L = 2 Ω		11		mV
	P_{OUT} = 5.2 W R_L = 4 Ω		55		mV
	P_{OUT} = 8 W R_L = 2 Ω		50		mV
Frequency Response (−3 dB)	R_L = 4 Ω C_{FB} = 39 nF R_{FB} = 39 Ω See Figs 15, 19		40–15000		Hz
Total Harmonic Distortion	A_V = 100 f = 1 kHz				
	P_{OUT} = 0.05-3.5 W (R_L = 4 Ω)		0.2		%
	P_{OUT} = 0.05-5 W (R_L = 2 Ω)		0.2		%
Input Resistance (Pin 1)	f = 1 kHz	70	150		kΩ
Voltage Gain					
(open loop)	f = 1 kHz R_L = 4 Ω		80		dB
(closed loop)		39.5	40	40.5	dB
Input Noise Voltage	BW (−3dB) = 40–15000 Hz Note 1		4		μV
Input Noise Current			60		pA
Efficiency	A_V = 100 f = 1 kHz				
	P_{OUT} = 5.2 W R_L = 4 Ω		68		%
	P_{OUT} = 8 W R_L = 4 Ω		58		%
Supply Voltage Rejection Ratio	AV = 100 R_L = 4 Ω R_g = 10 kΩ f_{ripple} = 100 Hz V_{ripple} = 0.5 V	30	35		dB

Note 1: Bandwidth (−3 dB) of test equipment = 10-25000 Hz

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TYPICAL PERFORMANCE CURVES

QUIESCENT OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE

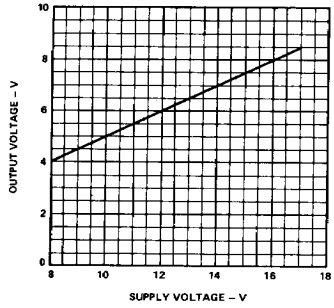

Fig. 1

QUIESCENT DRAIN CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

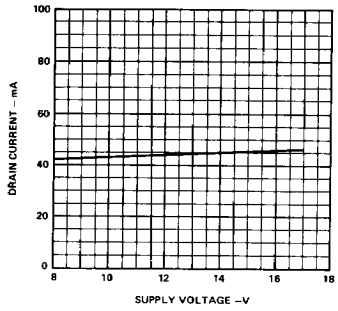

Fig. 2

OUTPUT POWER AS A FUNCTION OF SUPPLY VOLTAGE

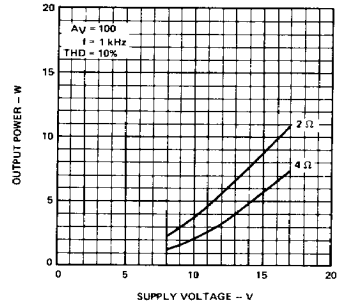

Fig. 3

OUTPUT POWER AS A FUNCTION OF LOAD RESISTANCE (RL)

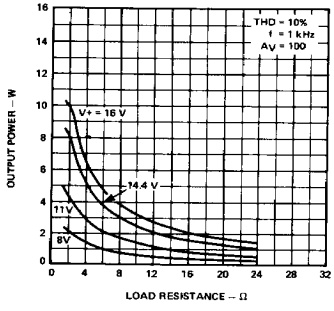

Fig. 4

INPUT VOLTAGE AS A FUNCTION OF VOLTAGE GAIN (R_L = 4 Ω)

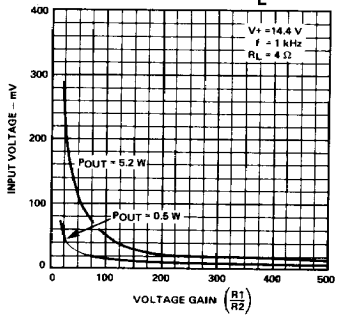

Fig. 5

INPUT VOLTAGE AS A FUNCTION OF VOLTAGE GAIN (R_L = 2 Ω)

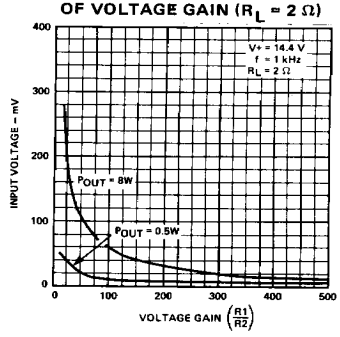

Fig. 6

TOTAL HARMONIC DISTORTION AS A FUNCTION OF OUTPUT POWER

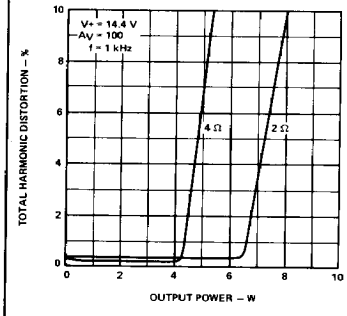

Fig. 7

TOTAL HARMONIC DISTORTORTION AS A FUNCTION OF FREQUENCY (R_L = 2 Ω; R_L = 4 Ω)

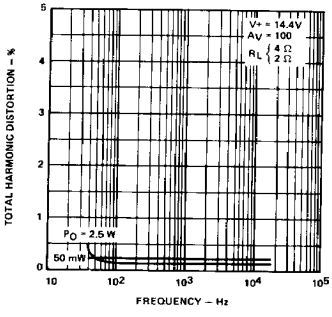

Fig. 8

SUPPLY VOLTAGE REJECTION AS A FUNCTION OF VOLTAGE GAIN

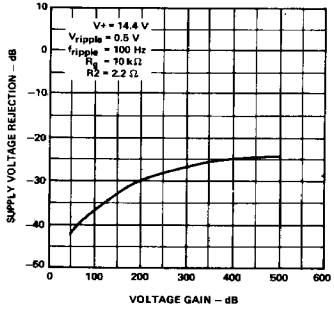

Fig. 9

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TYPICAL PERFORMANCE CURVES (Cont'd)

SUPPLY VOLTAGE REJECTION AS A FUNCTION OF FREQUENCY

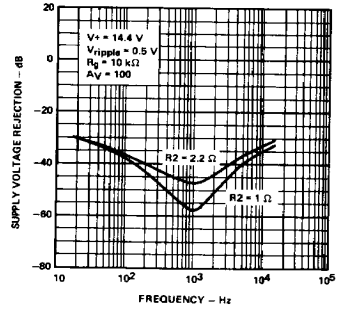

Fig. 10

POWER DISSIPATION AND EFFICIENCY AS A FUNCTION OF OUTPUT POWER (R_L = 4 Ω)

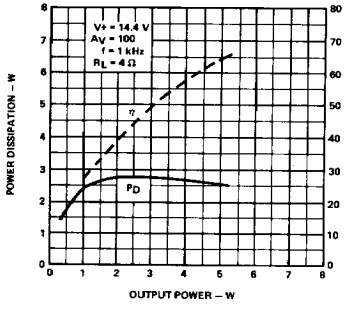

Fig. 11

POWER DISSIPATION AND EFFIECIENCY AS A FUNCTION OF OUTPUT POWER (R_L = 2 Ω)

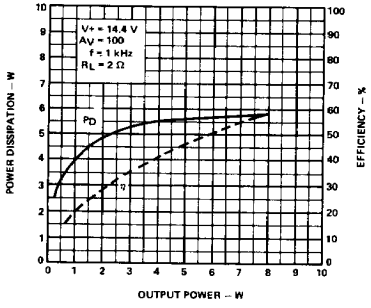

Fig. 12

MAXIMUM POWER DISSIPATION AS A FUNCTION OF SUPPLY VOLTAGE (SINE WAVE OPERATION)

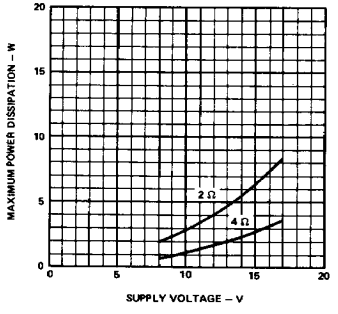

Fig. 13

MAXIMUM ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE

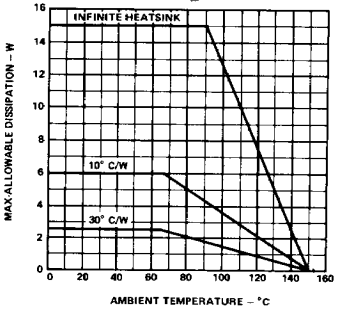

Fig. 14

CAPACITOR (CFB) AS A FUNCTION OF GAIN (VARIOUS BANDWIDTHS)

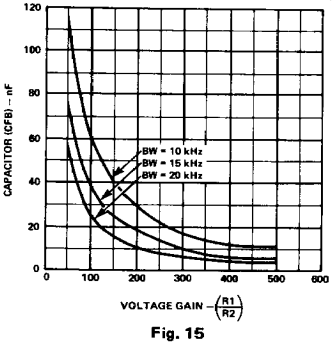

Fig. 15

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

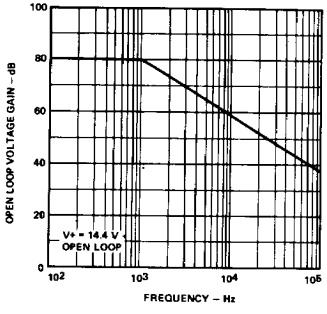

Fig. 16

OUTPUT POWER AND DRAIN CURRENT AS A FUNCTION OF CASE TEMPERATURE (R_L = 4 Ω)

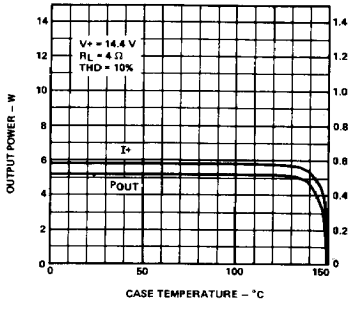

Fig. 17

OUTPUT POWER AND DRAIN CURRENT AS A FUNCTION OF CASE TEMPERATURE (R_L = 2 Ω)

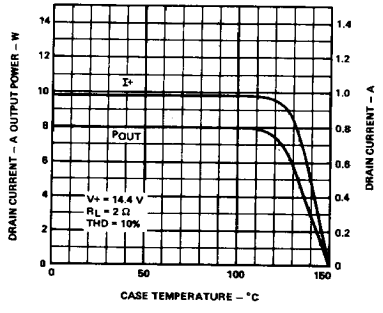

Fig. 18

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DESIGN CONSIDERATIONS

The board layout of the TDA2002 and TDA2002A is critical to assure good stability. The layout shown in Figure 20 is recommended. If a different layout is used, it is important that the ground points of inputs 1 and 2 be well decoupled from the ground of the output. Pin lengths should be as short as possible.

The component values shown on the applications schematics are recommended. However, other values may be used, and Table 1 is intended to serve as a guide for the designer on the effect of changing component values.

No electrical insulation is needed between the package tab and the heat sink, if the heat sink is electrically isolated or is at ground potential.

Component	Recommended value	Purpose	Larger than recommended value	Smaller than recommended value
C1	10 μF	Input DC decoupling		Noise at switch-on, switch-off
C2	470 μF	Ripple rejection		Degradation of PSRR
C3	0.1 μF	Supply bypassing		Danger of oscillation
C4	1000 μF	Output coupling to load		Higher low frequency cutoff
C5	0.1 μF	Frequency stability		Danger of oscillation at high frequencies with inductive loads
CF_B	$\simeq \frac{1}{2\pi B R 1}$	Upper frequency cutoff	Lower bandwidth	Larger bandwidth
R1	$(A_V - 1) \cdot R2$	Closed loop gain determination		Increase of drain current
R2	2.2 Ω	Closed loop gain and PSRR determination	Degradation of PSRR	
R3	1 Ω	Frequency stability	Danger of oscillation at high frequencies with inductive loads	
R_{FB}	$\cong$ 20 R2	Upper frequency cutoff	Poor high frequency attenuation	Danger of oscillation

TABLE 1

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APPLICATIONS INFORMATION:

Several typical applications of the TDA2002 and TDA2002A are shown in this section, together with printed circuit board layouts.

Figures 19 and 20 show a typical circuit with CFB, RFB shown dashed. CFB and RFB may be used to adjust the bandwidth after the gain has been set by the ratio R1/R2. (See Figure 15).

Figures 23 and 24 show a typical 15 watt bridge circuit utilizing two devices. A potentiometer (P1) is included to balance the offset voltages between the two devices.

TYPICAL APPLICATION CIRCUIT

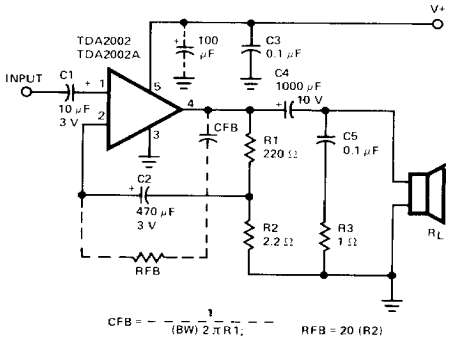

Fig. 19

P.C. BOARD AND COMPONENT LAYOUT FOR THE CIRCUIT OF FIG. 19 (1:1 SCALE)

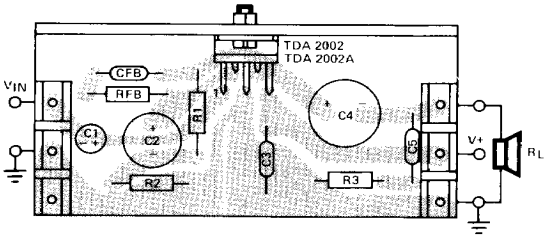

Fig. 20

LOW COST APPLICATION CIRCUIT

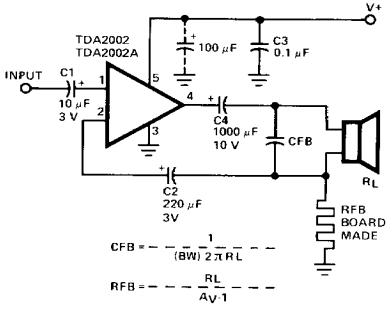

Fig. 21

P.C. BOARD AND COMPONENT LAYOUT FOR THE CIRCUIT OF FIG. 21 (1:1 SCALE)

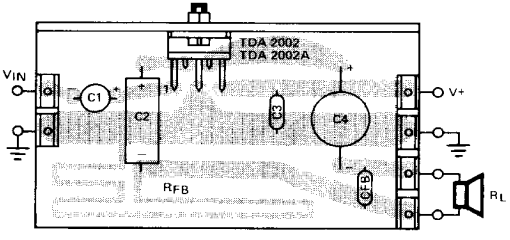

Fig. 22

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15 WATT BRIDGE CIRCUIT

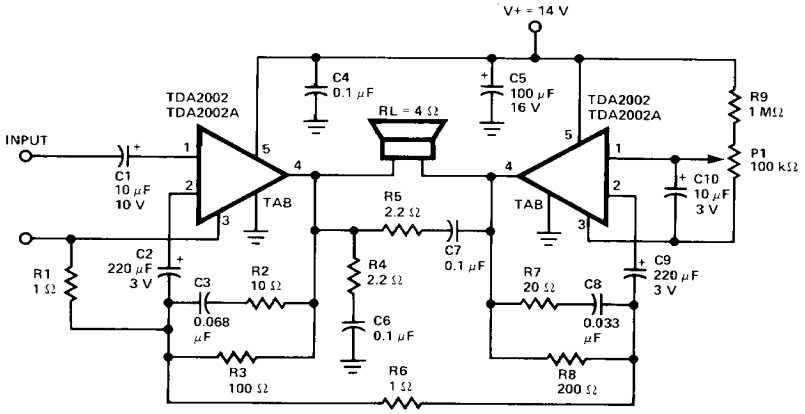

Fig. 23

P.C. BOARD AND COMPONENT LAYOUT FOR THE CIRCUIT OF FIG. 23 (1:1 SCALE)

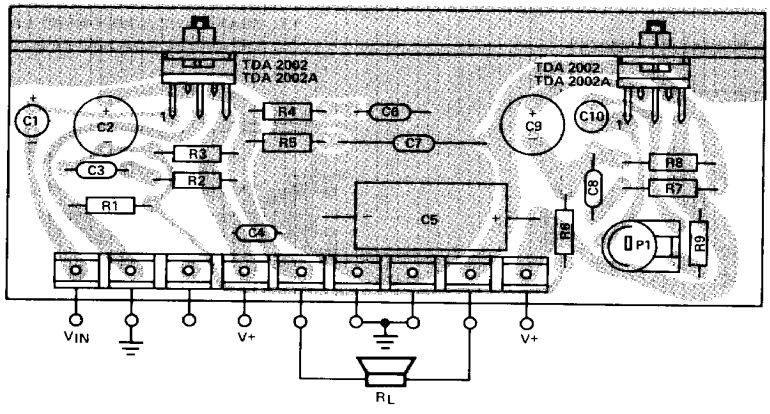

Fig. 24

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THERMAL SHUTDOWN

Both the TDA2002 and TDA2002A have been designed with a thermal shutdown feature. Typical curves of output power and supply current as a function of case temperature are shown in Figures 17 and 18. The thermal overload circuit reduces the drive to the output stage when the junction temperature exceeds the design threshold. The result is a reduced supply current and power output consistent with maintaining the junction temperature at the design limit.

The thermal overload feature offers several important advantages to the circuit designer:

1. The device can withstand excessive ambient temperatures (below 150° C) and temporary or permanent overloads on the output.
2. The safety margin on the heat sink design may be reduced because the device will not be damaged by excessive junction temperature (below 150° C). The only result of this increased junction temperature will be a reduction in output power and supply current.

OVERVOLTAGE (LOAD DUMP) PROTECTION

The TDA2002 has been designed with a built-in circuit which enables this device to withstand a series of voltage spikes (see Figure 25). The load dump feature starts at about 18 V, so the operating voltage must not exceed 18 V.

This feature is particularly important in automobile applications, and the pulse train shown in Figure 25 is intended to simulate the voltage spikes which often occur on the supply line in automotive applications.

If the supply voltage peaks exceed 40 V, then an LC network must be inserted between the supply and Pin 5 to assure that the pulses at Pin 5 will not exceed the limits shown in Figure 25. A typical LC network is shown in Figure 26. With this network a train of pulses up to 120 V and 2 ms wide can be applied from the supply line.

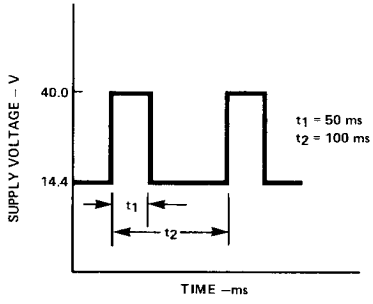


Fig. 25

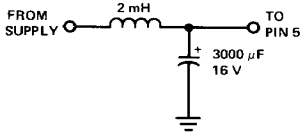
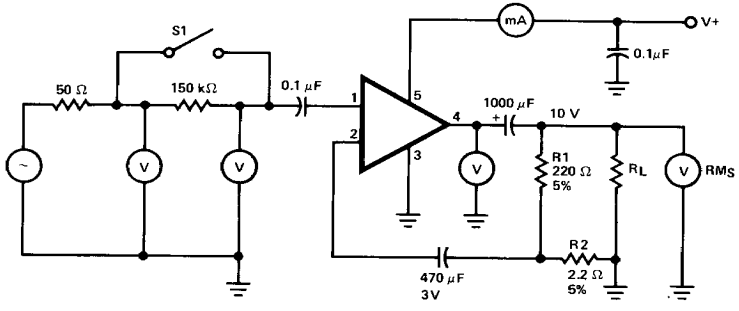


Fig. 26

TEST CIRCUIT



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